REMARKS

This is a full and timely response to the non-final Office action mailed October 20, 2004. Reexamination and reconsideration in view of the foregoing amendments and following remarks is respectfully solicited.

Claims 1-24 are now pending in this application, with Claims 1, 13, and 24 being the independent claims. Claims 1, 3, 5, 13, 16, and 24 have been amended, and Claims 25-53 have been canceled herein without prejudice or disclaimer of the subject matter, these latter claims having been withdrawn from consideration as being drawn to non-elected inventions. No new matter is believed to have been added.

Rejections Under 35 U.S.C. § 102

Claims 1-7, 13-18, and 24 were rejected under 35 U.S.C. § 102 as allegedly being anticipated by U.S. Patent No. 6,021,271 (Winter et al.). This rejection is respectfully traversed.

Independent Claims 1, 13, and 24 each relate to a method of verifying proper design and operation of a programmed programmable logic device (PLD) utilizing a PLD test device. The method defined by each of these independent claims includes developing at least one simulation test vector using a PLD design automation software tool, and testing a simulated model of the programmed PLD using each of the simulation test vectors, and each of these claims recites, *inter alia*, translating at least one simulation test vector into at least one device level test vector while testing the simulation test model, each device level test vector being in a format readable by the PLD test device.

Winter et al. relates to a method of verifying an electronic circuit design and discloses generating and processing a simulation input file that is used to test the circuit design, and generating a model file of the electronic design. A simulation program is then run using the processed simulation input file and the model file to generate a simulation results file. The simulation results file includes simulation test vectors and comment lines. When the simulation is completed, the simulation results file is reviewed to confirm the simulation was successful.

Once the simulation results file is reviewed, a test input file is generated by translating the simulation results file to a language used by a test machine. The test input file is then compiled by the tester, and is used to test actual circuits. The test input file generates test vectors in a test results file, which is then compared to corresponding test vectors in the simulation results file.

Hence, it is clear that Winter et al. fails to disclose (or even remotely suggest) at least the above-noted feature recited in independent Claims 1, 13, and 24. Namely, Winter et al. fails to disclose translating at least one simulation test vector into at least one device level test vector while testing the simulation test model. Indeed, Winter et al. explicitly discloses generating a test input file only after the simulation results file has been reviewed.

In view of the foregoing, reconsideration and withdrawal of the § 102 rejection is respectfully solicited.

Rejections Under 35 U.S.C. § 103

Claims 8 and 19 were rejected under 35 U.S.C. § 103 as allegedly being unpatentable over Winter et al., and Claims 9-12, and 20-23 were rejected under 35 U.S.C. § 103 as allegedly being unpatentable over Winter et al. and U.S. Patent No. 6,178,541 (Joly et al.) These rejections are respectfully traversed.

As was noted above, Winter et al. fails to disclose, or even remotely suggest, translating at least one simulation test vector into at least one device level test vector while testing the simulation test model. Moreover, Winter et al. explicitly teaches away from including such a feature, by teaching that a test input file is generated only after the simulation results file has been reviewed.

Joly et al. relates to a method of implementing integrated circuits using an iterative design process. However, this citation is not understood to make up for at least the above-noted deficiency of Winter et al.

Hence, Applicants respectfully request reconsideration and withdrawal of each of the § 103 rejections.

Conclusion

Based on the above, independent Claims 1, 13, and 24 are patentable over the citations of record. The dependent claims are also submitted to be patentable for the reasons given above with respect to the independent claims and because each recite features which are patentable in its own right. Individual consideration of the dependent claims is respectfully solicited.

The other art of record is also not understood to disclose or suggest the inventive concept of the present invention as defined by the claims.

Hence, Applicant submits that the present application is in condition for allowance. Favorable reconsideration and withdrawal of the objections and rejections set forth in the above-noted Office Action, and an early Notice of Allowance are requested.

If the Examiner has any comments or suggestions that could place this application in even better form, the Examiner is requested to telephone the undersigned attorney at the below-listed number.

If for some reason Applicant has not paid a sufficient fee for this response, please consider this as authorization to charge Ingrassia, Fisher & Lorenz, Deposit Account No. 50-2091 for any fee which may be due.

Respectfully submitted,

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